800 MHz Clock Distribution IC, Dividers, Delay Adjust, Three Outputs

AD9513

FEATURES

- **1.6 GHz differential clock input**
- **3 programmable dividers**
  - **Divide-by in range from1 to 32**
  - **Phase select for coarse delay adjust**
- **Three 800 MHz/250 MHz LVDS/CMOS clock outputs**
  - **Additive output jitter 300 fs rms**
  - **Time delays up to 11.6 ns**
- **Device configured with 4-level logic pins**
- **Space-saving, 32-lead LFCSP**

APPLICATIONS

- **Low jitter, low phase noise clock distribution**
- **Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs**
- **High performance wireless transceivers**
- **High performance instrumentation**
- **Broadband infrastructure**
- **ATE**

FUNCTIONAL BLOCK DIAGRAM

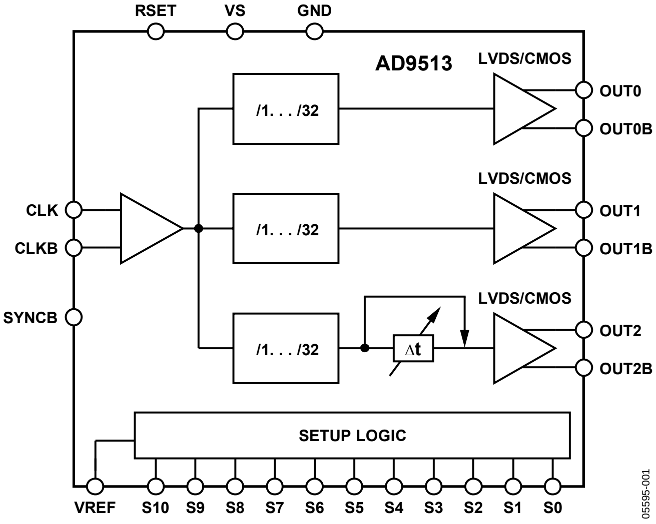


Figure 1.

GENERAL DESCRIPTION

The AD9513 features a three-output clock distribution IC in a design that emphasizes low jitter and phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

There are three independent clock outputs that can be set to either LVDS or CMOS levels. These outputs operate to 800 MHz in LVDS mode and to 250 MHz in CMOS mode.

Each output has a programmable divider that can be set to divide by a selected set of integers ranging from 1 to 32. The phase of one clock output relative to the other clock output can be set by means of a divider phase select function that serves as a coarse timing adjustment.

One of the outputs features a delay element with three selectable full-scale delay values (1.8 ns, 6.0 ns, and 11.6 ns), each with 16 steps of fine adjustment.

The AD9513 does not require an external controller for operation or setup. The device is programmed by means of 11 pins (S0 to S10) using 4-level logic. The programming pins are internally biased to ⅓ V_S. The VREF pin provides a level of ⅔ V_S. V_S (3.3 V) and GND (0 V) provide the other two logic levels.

The AD9513 is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

The AD9513 is available in a 32-lead LFCSP and operates from a single 3.3 V supply. The temperature range is −40°C to +85°C.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

9/05—Revision 0: Initial Version

SPECIFICATIONS

Typical (typ) is given for $V_S = 3.3\ V \pm 5\%$; $T_A = 25°C$, $R_{SET} = 4.12\ k\Omega$, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

CLOCK INPUT

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUT (CLK)					
Input Frequency	0		1.6	GHz	
Input Sensitivity[1]		150		mV p-p	
Input Common-Mode Voltage, V_{CM}	1.5	1.6	1.7	V	Self-biased; enables ac coupling
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Sensitivity, Single-Ended		150		mV p-p	CLK ac-coupled; CLKB ac-bypassed to RF ground
Input Resistance	4.0	4.8	5.6	kΩ	Self-biased
Input Capacitance		2		pF	

[1] A slew rate of 1 V/ns is required to meet jitter, phase noise, and propagation delay specifications.

CLOCK OUTPUTS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS CLOCK OUTPUT					Termination = 100 Ω differential
Differential					
Output Frequency	0		800	MHz	
Differential Output Voltage (V_{OD})	250	350	450	mV	
Delta V_{OD}			30	mV	
Output Offset Voltage (V_{OS})	1.125	1.23	1.375	V	
Delta V_{OS}			25	mV	
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND
CMOS CLOCK OUTPUT					Single-ended measurements; termination open
Single-Ended					Complementary output on (OUT1B)
Output Frequency	0		250	MHz	With 5 pF load
Output Voltage High (V_{OH})	$V_S - 0.1$			V	@ 1 mA load
Output Voltage Low (V_{OL})			0.1	V	@ 1 mA load

TIMING CHARACTERISTICS

CLK input slew rate = 1 V/ns or greater.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS					Termination = 100 Ω differential
Output Rise Time, t_{RL}		200	350	ps	20% to 80%, measured differentially
Output Fall Time, t_{FL}		210	350	ps	80% to 20%, measured differentially
PROPAGATION DELAY, t_{LVDS}, CLK-TO-LVDS OUT					Delay off on OUT2
OUT0, OUT1, OUT2					
Divide = 1	1.03	1.29	1.62	ns	
Divide = 2 – 32	1.09	1.35	1.68	ns	
Variation with Temperature		0.9		ps/°C	
OUT2					
Divide = 1	1.07	1.35	1.69	ns	
Divide = 2 – 32	1.13	1.41	1.75	ns	
Variation with Temperature		0.9		ps/°C	
OUTPUT SKEW, LVDS OUTPUTS					Delay off on OUT2
OUT0 to OUT1 on Same Part, t_{SKV} [1]	−135	−20	+125	ps	
OUT0 to OUT2 on Same Part, t_{SKV}[1]	−205	−65	+90	ps	
All LVDS OUTs Across Multiple Parts, t_{SKV_AB} [2]			375	ps	
Same LVDS OUTs Across Multiple Parts, t_{SKV_AB}[2]			300	ps	
CMOS					B outputs are inverted; termination = open
Output Rise Time, t_{RC}		650	865	ps	20% to 80%; C_{LOAD} = 3 pF
Output Fall Time, t_{FC}		650	990	ps	80% to 20%; C_{LOAD} = 3 pF
PROPAGATION DELAY, t_{CMOS}, CLK-TO-CMOS OUT					Delay off on OUT2
OUT0, OUT1					
Divide = 1	1.14	1.46	1.89	ns	
Divide = 2 – 32	1.19	1.51	1.94	ns	
Variation with Temperature		1		ps/°C	
OUT2					
Divide = 1	1.20	1.53	1.97	ns	
Divide = 2 – 32	1.24	1.57	2.01	ns	
Variation with Temperature		1		ps/°C	
OUTPUT SKEW, CMOS OUTPUTS					Delay off on OUT2
All CMOS OUTs on Same Part, t_{SKC}[1]	−230		+135	ps	
All CMOS OUTs Across Multiple Parts, t_{SKC_AB}[2]			415	ps	
Same CMOS OUTs Across Multiple Parts, t_{SKC_AB}[2]			330	ps	
LVDS-TO-CMOS OUT					Everything the same; different logic type
Output Skew, t_{SKV_C}			510	ps	LVDS to CMOS on same part
DELAY ADJUST (OUT2; LVDS AND CMOS)					
S0 = 1/3					
Zero-Scale Delay Time[3]		0.35		ns	
Zero-Scale Variation with Temperature		0.20		ps/°C	
Full-Scale Time Delay[3]		1.8		ns	
Full-Scale Variation with Temperature		−0.38		ps/°C	
S0 = 2/3					
Zero-Scale Delay Time[3]		0.48		ns	
Zero-Scale Variation with Temperature		0.31		ps/°C	
Full-Scale Time Delay[3]		6.0		ns	
Full-Scale Variation with Temperature		−1.3		ps/°C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
S0 = 1					
Zero-Scale Delay Time[3]		0.59		ns	
Zero-Scale Variation with Temperature		0.47		ps/°C	
Full-Scale Time Delay[3]		11.6		ns	
Full-Scale Variation with Temperature		−5		ps/°C	
Linearity, DNL		0.2		LSB	
Linearity, INL		0.2		LSB	

[1] This is the difference between any two similar delay paths within a single device operating at the same voltage and temperature.
[2] This is the difference between any two similar delay paths across multiple devices operating at the same voltage and temperature.
[3] Incremental delay; does not include propagation delay.

CLOCK OUTPUT PHASE NOISE

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVDS ADDITIVE PHASE NOISE					
CLK = 622.08 MHz, OUT = 622.08 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−100		dBc/Hz	
@ 100 Hz Offset		−110		dBc/Hz	
@ 1 kHz Offset		−118		dBc/Hz	
@ 10 kHz Offset		−129		dBc/Hz	
@ 100 kHz Offset		−135		dBc/Hz	
@ 1 MHz Offset		−140		dBc/Hz	
>10 MHz Offset		−148		dBc/Hz	
CLK = 622.08 MHz, OUT = 155.52 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−112		dBc/Hz	
@ 100 Hz Offset		−122		dBc/Hz	
@ 1 kHz Offset		−132		dBc/Hz	
@ 10 kHz Offset		−142		dBc/Hz	
@ 100 kHz Offset		−148		dBc/Hz	
@ 1 MHz Offset		−152		dBc/Hz	
>10 MHz Offset		−155		dBc/Hz	
CLK = 491.52 MHz, OUT = 245.76 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−108		dBc/Hz	
@ 100 Hz Offset		−118		dBc/Hz	
@ 1 kHz Offset		−128		dBc/Hz	
@ 10 kHz Offset		−138		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−148		dBc/Hz	
>10 MHz Offset		−154		dBc/Hz	
CLK = 491.52 MHz, OUT = 122.88 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−118		dBc/Hz	
@ 100 Hz Offset		−129		dBc/Hz	
@ 1 kHz Offset		−136		dBc/Hz	
@ 10 kHz Offset		−147		dBc/Hz	
@ 100 kHz Offset		−153		dBc/Hz	
@ 1 MHz Offset		−156		dBc/Hz	
>10 MHz Offset		−158		dBc/Hz	
CLK = 245.76 MHz, OUT = 245.76 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−108		dBc/Hz	
@ 100 Hz Offset		−118		dBc/Hz	
@ 1 kHz Offset		−128		dBc/Hz	
@ 10 kHz Offset		−138		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−148		dBc/Hz	
>10 MHz Offset		−155		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK = 245.76 MHz, OUT = 122.88 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−118		dBc/Hz	
@ 100 Hz Offset		−127		dBc/Hz	
@ 1 kHz Offset		−137		dBc/Hz	
@ 10 kHz Offset		−147		dBc/Hz	
@ 100 kHz Offset		−154		dBc/Hz	
@ 1 MHz Offset		−156		dBc/Hz	
>10 MHz Offset		−158		dBc/Hz	
CLK-TO-CMOS ADDITIVE PHASE NOISE					
CLK = 245.76 MHz, OUT = 245.76 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−110		dBc/Hz	
@ 100 Hz Offset		−121		dBc/Hz	
@ 1 kHz Offset		−130		dBc/Hz	
@ 10 kHz Offset		−140		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−149		dBc/Hz	
>10 MHz Offset		−156		dBc/Hz	
CLK = 245.76 MHz, OUT = 61.44 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−125		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−143		dBc/Hz	
@ 10 kHz Offset		−152		dBc/Hz	
@ 100 kHz Offset		−158		dBc/Hz	
@ 1 MHz Offset		−160		dBc/Hz	
>10 MHz Offset		−162		dBc/Hz	
CLK = 78.6432 MHz, OUT = 78.6432 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−122		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−140		dBc/Hz	
@ 10 kHz Offset		−150		dBc/Hz	
@ 100 kHz Offset		−155		dBc/Hz	
@ 1 MHz Offset		−158		dBc/Hz	
>10 MHz Offset		−160		dBc/Hz	
CLK = 78.6432 MHz, OUT = 39.3216 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−128		dBc/Hz	
@ 100 Hz Offset		−136		dBc/Hz	
@ 1 kHz Offset		−146		dBc/Hz	
@ 10 kHz Offset		−155		dBc/Hz	
@ 100 kHz Offset		−161		dBc/Hz	
>1 MHz Offset		−162		dBc/Hz	

CLOCK OUTPUT ADDITIVE TIME JITTER

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT ADDITIVE TIME JITTER					Calculated from SNR of ADC method
CLK= 400 MHz		300		fs rms	
LVDS (OUT0) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT1, OUT2) = 100 MHz					Interferer
CLK = 400 MHz		300		fs rms	
LVDS (OUT0) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT1, OUT2) = 50 MHz					Interferer
CLK = 400 MHz		305		fs rms	
LVDS (OUT1) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT0, OUT2) = 100 MHz					Interferer
CLK = 400 MHz		310		fs rms	
LVDS (OUT1) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT0, OUT2) = 50 MHz					Interferer
CLK = 400 MHz		310		fs rms	
LVDS (OUT2) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT0, OUT1) = 100 MHz					Interferer
CLK = 400 MHz		315		fs rms	
LVDS (OUT2) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT0, OUT1) = 50 MHz					Interferer
CLK = 400 MHz		345		fs rms	
LVDS (OUT2) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT0, OUT1) = 50 MHz					Interferer
CMOS OUTPUT ADDITIVE TIME JITTER					Calculated from SNR of ADC method
CLK = 400 MHz		300		fs rms	
CMOS (OUT0) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT2) = 100 MHz					Interferer
CLK = 400 MHz		300		fs rms	
CMOS (OUT0) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT1, OUT2) = 50 MHz					Interferer
CLK = 400 MHz		335		fs rms	
CMOS (OUT1) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT0, OUT2) = 50 MHz					Interferer
CLK = 400 MHz		355		fs rms	
CMOS (OUT2) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT0, OUT1) = 50 MHz					Interferer
CLK = 400 MHz		340		fs rms	
CMOS (OUT2) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT0, OUT1) = 50 MHz					Interferer

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DELAY BLOCK ADDITIVE TIME JITTER[1]					100 MHz output; incremental additive jitter[1]
Delay FS = 1.8 ns Fine Adj. 00000		0.71		ps rms	
Delay FS = 1.8 ns Fine Adj. 11111		1.2		ps rms	
Delay FS = 6.0 ns Fine Adj. 00000		1.3		ps rms	
Delay FS = 6.0 ns Fine Adj. 11111		2.7		ps rms	
Delay FS = 11.6 ns Fine Adj. 00000		2.0		ps rms	
Delay FS = 11.6 ns Fine Adj. 11111		2.8		ps rms	

[1] This value is incremental. That is, it is in addition to the jitter of the LVDS or CMOS output without the delay. To estimate the total jitter, the LVDS or CMOS output jitter should be added to this value using the root sum of the squares (RSS) method.

SYNCB, VREF, AND SETUP PINS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYNCB					
Logic High	2.7			V	
Logic Low			0.40	V	
Capacitance		2		pF	
VREF					
Output Voltage	$0.62 \cdot V_S$		$0.76 \cdot V_S$	V	Minimum – maximum from 0 mA to 1 mA load
S0 TO S10					
Levels					
0			$0.1 \cdot V_S$	V	
1/3	$0.2 \cdot V_S$		$0.45 \cdot V_S$	V	
2/3	$0.55 \cdot V_S$		$0.8 \cdot V_S$	V	
1	$0.9 \cdot V_S$			V	

POWER

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-ON SYNCHRONIZATION[1] V_S Transit Time from 2.2 V to 3.1 V			35	ms	See the Power-On SYNC section.
POWER DISSIPATION	175	325	575	mW	All three outputs on. LVDS (divide = 2). No clock. Does not include power dissipated in external resistors.
	240	460	615	mW	All three outputs on. CMOS (divide = 2); 62.5 MHz out (5 pF load).
	320	605	840	mW	All three outputs on. CMOS (divide = 2); 125 MHz out (5 pF load).
POWER DELTA					
Divider (Divide = 2 to Divide = 1)	15	30	45	mW	For each divider. No clock.
LVDS Output	20	50	85	mW	No clock.
CMOS Output (Static)	30	40	50	mW	No clock.
CMOS Output (@ 62.5 MHz)	65	110	155	mW	Single-ended. At 62.5 MHz out with 5 pF load.
CMOS Output (@ 125 MHz)	70	145	220	mW	Single-ended. At 125 MHz out with 5 pF load.
Delay Block	30	45	65	mW	Off to 1.8 ns fs, delay word = 60; output clocking at 62.5 MHz.

[1] This is the rise time of the V_S supply that is required to ensure that a synchronization of the outputs occurs on power-up. The critical factor is the time it takes the V_S to transition the range from 2.2 V to 3 .1 V. If the rise time is too slow, the outputs are not synchronized.

TIMING DIAGRAMS

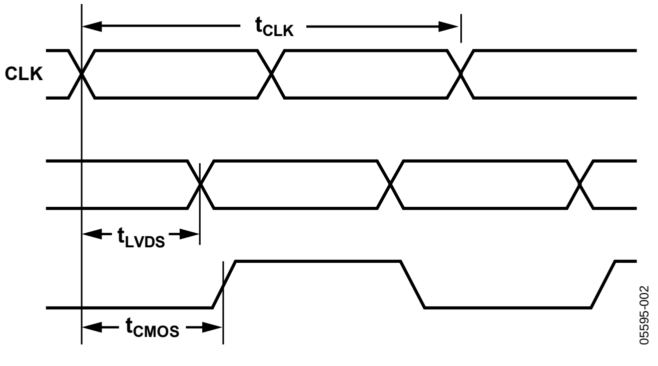


Figure 2. CLK/CLKB to Clock Output Timing, DIV = 1 Mode

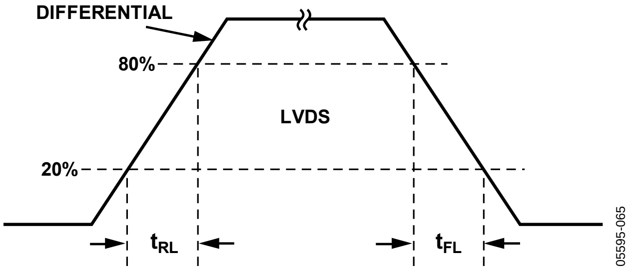


Figure 3. LVDS Timing, Differential

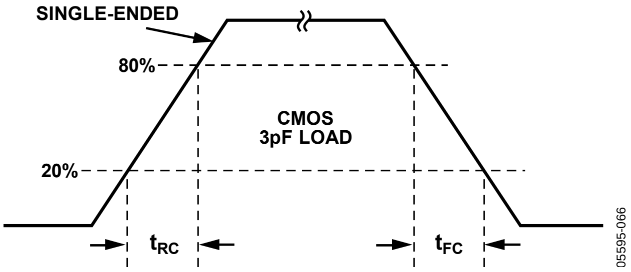


Figure 4. CMOS Timing, Single-Ended, 3 pF Load

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter or Pin	With Respect to	Min	Max	Unit
VS	GND	−0.3	+3.6	V
RSET	GND	−0.3	$V_S + 0.3$	V
CLK	GND	−0.3	$V_S + 0.3$	V
CLK	CLKB	−1.2	+1.2	V
OUT0, OUT1, OUT2	GND	−0.3	$V_S + 0.3$	V
FUNCTION	GND	−0.3	$V_S + 0.3$	V
STATUS	GND	−0.3	$V_S + 0.3$	V
Junction Temperature[1]			150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS[2]

Thermal Resistance

32-Lead LFCSP[3]
$\theta_{JA} = 36.6°C/W$

---

[1] See Thermal Characteristics for θ_{JA}.
[2] Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-7.
[3] The external pad of this package must be soldered to adequate copper land on board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

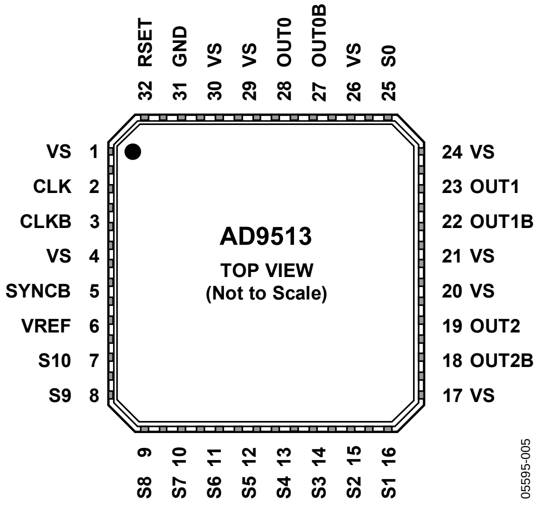


Figure 5. 32-Lead LFCSP Pin Configuration

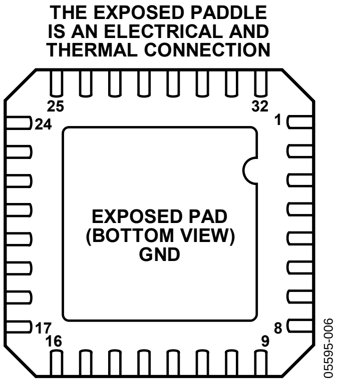


Figure 6. Exposed Paddle

Note that the exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle *must* be soldered to a PCB land that functions as both a heat dissipation path as well as an electrical ground.

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4 ,17 ,20, 21, 24, 26, 29, 30	VS	Power Supply (3.3 V).
2	CLK	Clock Input.
3	CLKB	Complementary Clock Input.
5	SYNCB	Used to Synchronize Outputs.
6	VREF	Provides 2/3 V_S for use as one of the four logic levels on S0 to S10.
7 to16, 25	S10 to S1, S0	Setup Select Pins. These are 4-state logic. The logic levels are V_S, GND, 1/3 V_S, and 2/3 V_S. The VREF pin provides 2/3 V_S. Each pin is internally biased to 1/3 V_S so that a pin requiring that logic level should be left NC (no connection).
18	OUT2B	Complementary LVDS/Inverted CMOS Output.
19	OUT2	LVDS/CMOS Output.
22	OUT1B	Complementary LVDS/Inverted CMOS Output. OUT6 includes a delay block.
23	OUT1	LVDS/CMOS Output. OUT6 includes a delay block.
27	OUT0B	Complementary LVDS/Inverted CMOS Output. OUT5 includes a delay block.
28	OUT0	LVDS/CMOS Output. OUT5 includes a delay block.
31	GND	Ground. The exposed paddle on the back of the chip is also GND.
32	RSET	Current Set Resistor to Ground. Nominal value = 4.12 kΩ.

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0 to 360 degrees for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although there are many causes that can contribute to phase jitter, one major component is due to random noise that is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is also meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings is seen to vary. For a square wave, the time jitter is seen as a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Since these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the SNR and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

It is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources has been subtracted. This makes it possible to predict the degree to which the device as the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contribute their own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise.

Additive Time Jitter

It is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources has been subtracted. This makes it possible to predict the degree to which the device will affect the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contribute their own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

TYPICAL PERFORMANCE CHARACTERISTICS

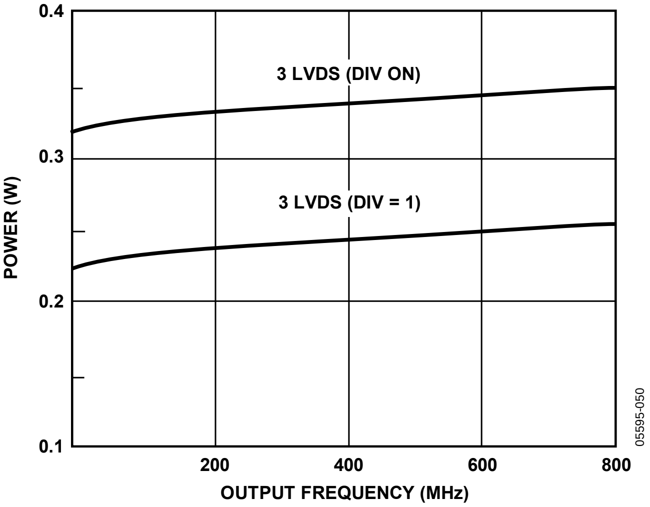


Figure 7. Power vs. Frequency—LVDS

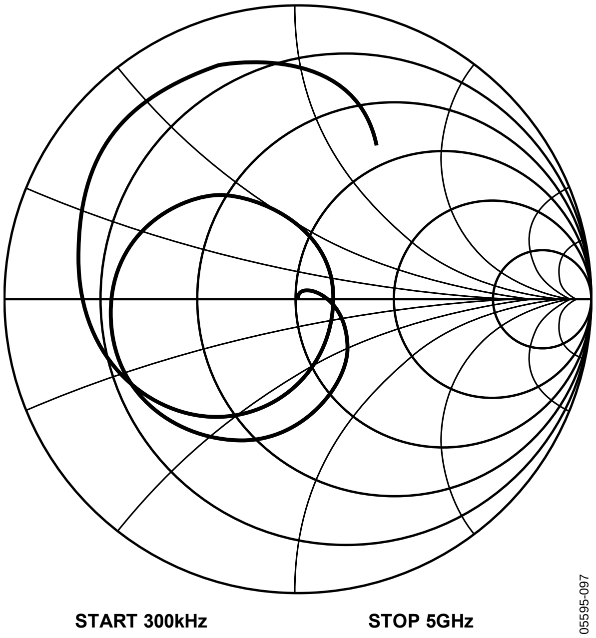


Figure 8. CLK Smith Chart (Evaluation Board)

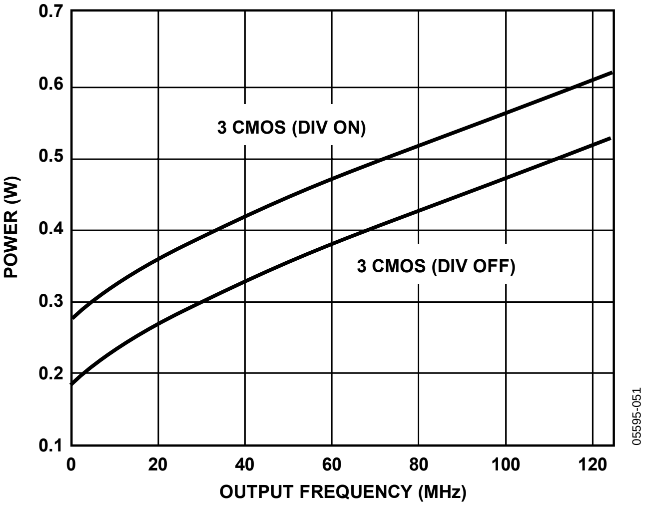


Figure 9. Power vs. Frequency—CMOS

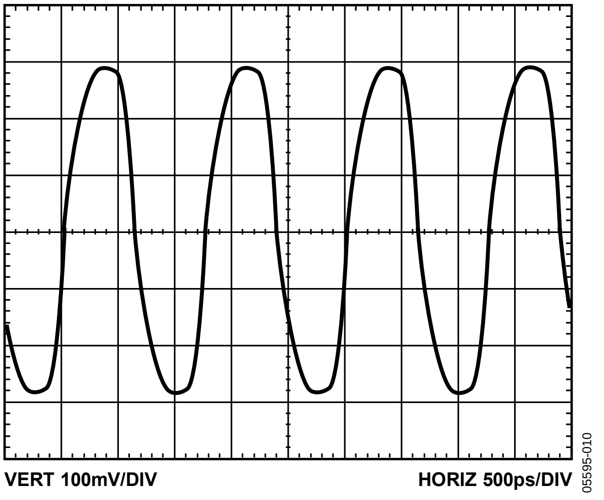


Figure 10. LVDS Differential Output @ 800 MHz

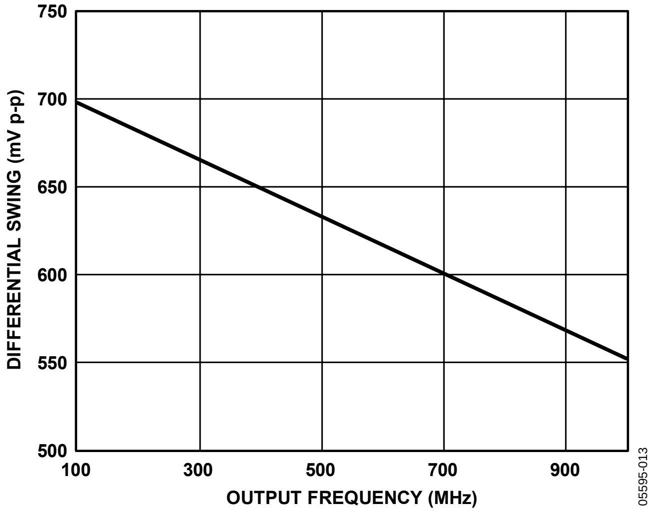


Figure 12. LVDS Differential Output Swing vs. Frequency

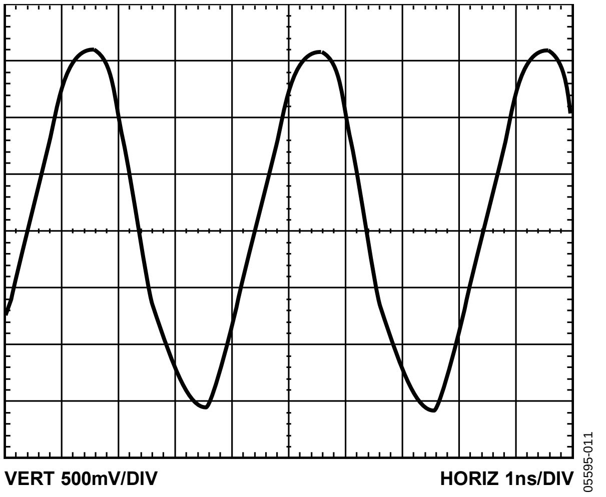


Figure 11. CMOS Single-Ended Output @ 250 MHz with 10 pF Load

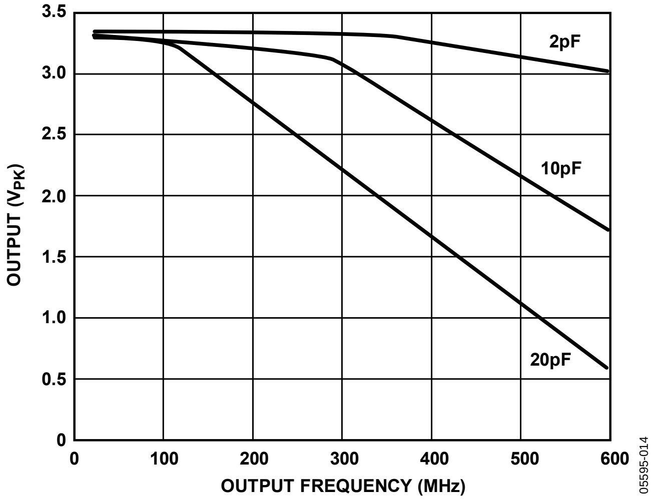


Figure 13. CMOS Single-Ended Output Swing vs. Frequency and Load

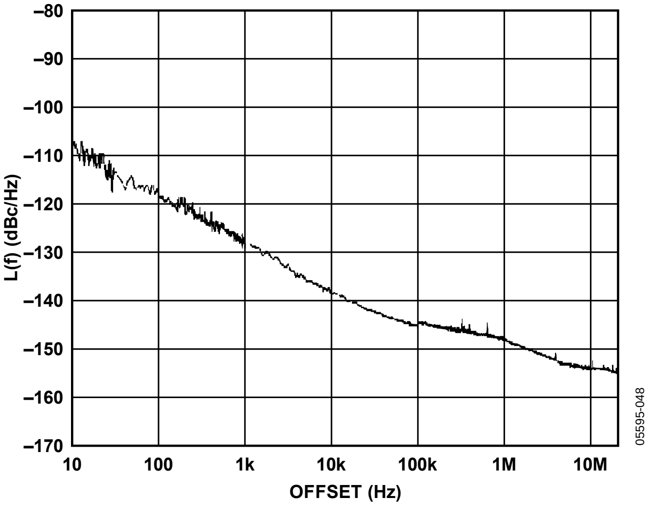


Figure 14. Additive Phase Noise—LVDS DIV 1, 245.76 MHz

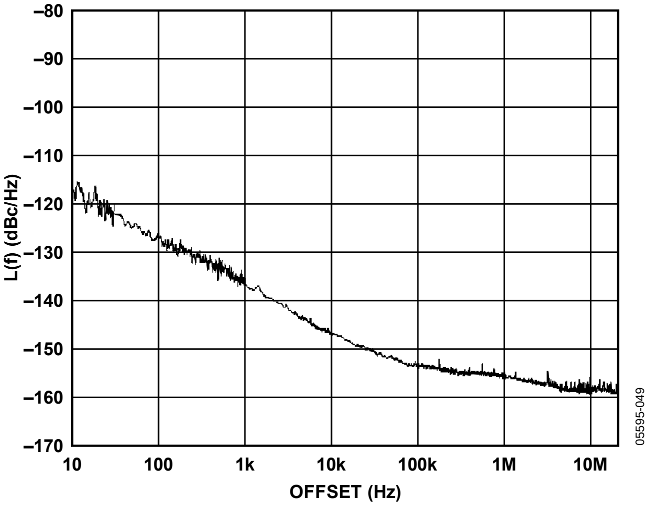


Figure 16. Additive Phase Noise—LVDS DIV2, 122.88 MHz

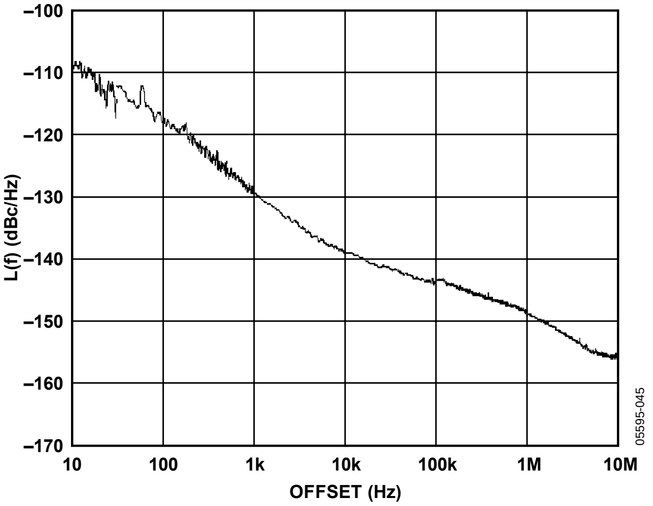


Figure 15. Additive Phase Noise—CMOS DIV 1, 245.76 MHz

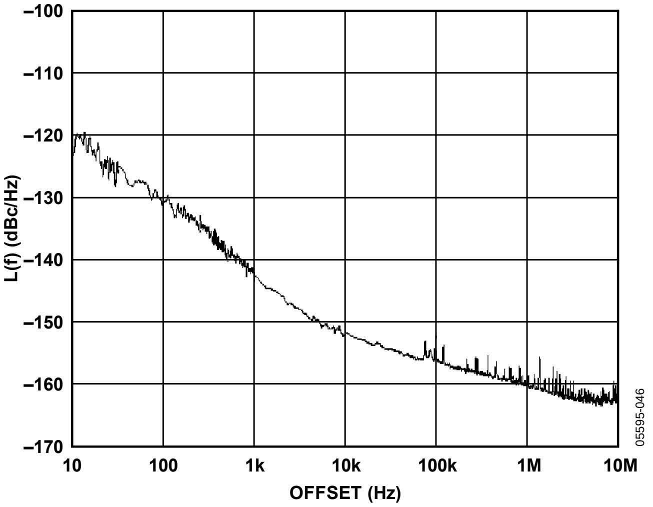


Figure 17. Additive Phase Noise—CMOS DIV4, 61.44 MHz

FUNCTIONAL DESCRIPTION

OVERALL

The AD9513 provides for the distribution of its input clock on up to three outputs. Each output can be set to either LVDS or CMOS logic levels. Each output has its own divider that can be set for a divide ratio selected from a list of integer values from 1 (bypassed) to 32.

OUT2 includes an analog delay block that can be set to add an additional delay of 1.8 ns, 6.0 ns, or 11.6 ns full scale, each with 16 levels of fine adjustment.

CLK, CLKB—DIFFERENTIAL CLOCK INPUT

The CLK and CLKB pins are differential clock input pins. This input works up to 1600 MHz. The jitter performance is degraded by a slew rate below 1 V/ns. The input level should be between approximately 150 mV p-p to no more than 2 V p-p. Anything greater can result in turning on the protection diodes on the input pins.

See Figure 18 for the CLK equivalent input circuit. This input is fully differential and self-biased. The signal should be ac-coupled using capacitors. If a single-ended input must be used, this can be accommodated by ac coupling to one side of the differential input only. The other side of the input should be bypassed to a quiet ac ground by a capacitor.

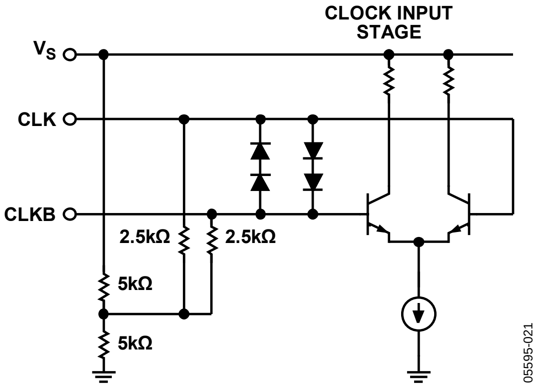


Figure 18. Clock Input Equivalent Circuit

SYNCHRONIZATION

Power-On SYNC

A power-on sync (POS) is issued when the V_S power supply is turned on to ensure that the outputs start in synchronization. The power-on sync works only if the V_S power supply transitions the region from 2.2 V to 3.1 V within 35 ms. The POS can occur up to 65 ms after V_S crosses 2.2 V. Only outputs which are not divide = 1 are synchronized.

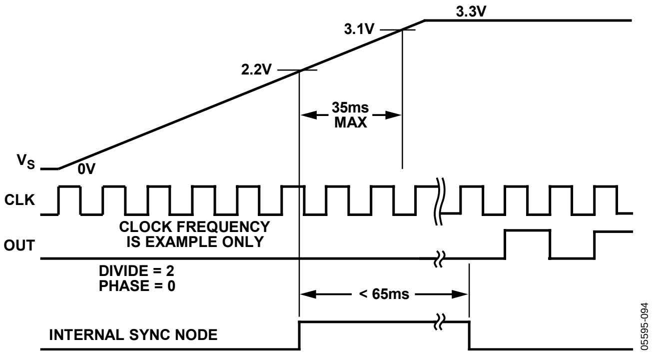


Figure 19. Power-On Sync Timing

SYNCB

If the setup configuration of the AD9513 is changed during operation, the outputs can become unsynchronized. The outputs can be resynchronized to each other at any time. Synchronization occurs when the SYNCB pin is pulled low and released. The clock outputs (except where divide = 1) are forced into a fixed state (determined by the divide and phase settings) and held there in a static condition, until the SYNCB pin is returned to high. Upon release of the SYNCB pin, after four cycles of the clock signal at CLK, all outputs continue clocking in synchronicity (except where divide = 1).

When divide = 1 for an output, that output is not affected by SYNCB.

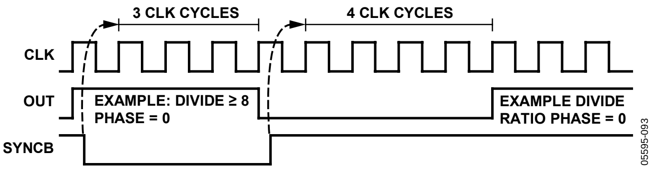


Figure 20. SYNCB Timing with Clock Present

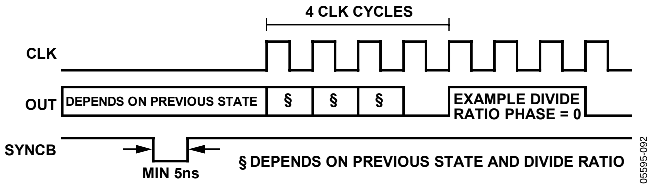


Figure 21. SYNCB Timing with No Clock Present

The outputs of the AD9513 can be synchronized by using the SYNCB pin. Synchronization aligns the phases of the clock outputs, respecting any phase offset that has been set on an output's divider.

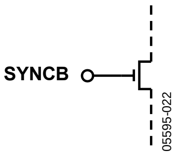


Figure 22. SYNCB Equivalent Input Circuit

Synchronization is initiated by pulling the SYNCB pin low for a minimum of 5 ns. The input clock does not have to be present at the time the command is issued. The synchronization occurs after four input clock cycles.

The synchronization applies to clock outputs

- that are not turned OFF
- where the divider is not divide = 1 (divider bypassed)

An output with its divider set to divide = 1 (divider bypassed) is always synchronized with the input clock, with a propagation delay.

The SYNCB pin must be pulled up for normal operation. Do not let the SYNCB pin float.

RSET RESISTOR

The internal bias currents of the AD9513 are set by the R_{SET} resistor. This resistor should be as close as possible to the value given as a condition in the Specifications section (R_{SET} = 4.12 kΩ). This is a standard 1% resistor value and should be readily obtainable. The bias currents set by this resistor determine the logic levels and operating conditions of the internal blocks of the AD9513. The performance figures given in the Specifications section assume that this resistor value is used for R_{SET}.

VREF

The VREF pin provides a voltage level of ⅔ V_S. This voltage is one of the four logic levels used by the setup pins (S0 to S10). These pins set the operation of the AD9513. The VREF pin provides sufficient drive capability to drive as many of the setup pins as necessary, up to all on a single part. The VREF pin should be used for no other purpose.

SETUP CONFIGURATION

The specific operation of the AD9513 is set by the logic levels applied to the setup pins (S10 to S0). These pins use four-state logic. The logic levels used are V_S and GND, plus ⅓ V_S and ⅔ V_S. The ⅓ V_S level is provided by the internal self-biasing on each of the setup pins (S10 to S0). This is the level seen by a setup pin that is left not connected (NC). The ⅔ V_S level is provided by the VREF pin. All setup pins requiring the ⅔V_S level must be tied to the VREF pin.

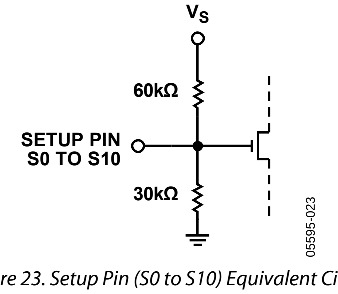


Figure 23. Setup Pin (S0 to S10) Equivalent Circuit

The AD9513 operation is determined by the combination of logic levels present at the setup pins. The setup configurations for the AD9513 are shown in Table 11 to Table 16. The four logic levels are referred to as 0, ⅓, ⅔, and 1. These numbers represent the fraction of the V_S voltage that defines the logic levels. See the setup pin thresholds in Table 6.

The meaning of some of the pin settings is changed by the settings of other pins. For example, S0 determines whether S3, and S4 sets OUT2 delay (S0 ≠ 0) or OUT2 phase (S0 = 0).

S2 indicates which outputs are in use, as shown in Table 10. This allows the same pins (S5 and S6, S7 and S8) to determine the settings for two different outputs, depending on which outputs are in use.

Table 10. S2 Indicates Which Outputs Are in Use

S2	Outputs
0	OUT2 Off
1/3	All Outputs On
2/3	OUT0 Off
1	OUT1 Off

The fine delay values set by S3 and S4 (when the delay is being used, S0 ≠ 0) are fractions of the full-scale delay. Note that the longest setting is 15/16 of full scale. The full-scale delay times are given in Table 3. To determine the actual delay, take the fraction corresponding to the fine delay setting and multiply by the full-scale value set by Table 3 corresponding to the S0 value and add the LVDS or CMOS propagation delay time (see Table 3). The full-scale delay times shown in Table 11, and referred to elsewhere, are nominal time values.

The value at S2 also determines whether S5 and S6 set OUT2 divide (S2 ≠ 0) or OUT1 phase (S2 = 0). In addition, S2 determines whether S7 and S8 set OUT1 divide (S2 ≠ 1) or OUT2 phase (S2 = 1 and S0 ≠ 0). In addition, the value of S2 determines whether S9 and S10 set OUT0 divide (S2 ≠ 2/3) or OUT2 divide (S2 = 2/3).

Table 11. Output Delay Full Scale

S0	Delay
0	Bypass
1/3	1.8 ns
2/3	6.0 ns
1	11.6 ns

Table 12. Output Logic Configuration

S1	S2	OUT0	OUT1	OUT2
0	0	OFF	LVDS	OFF
1/3	0	CMOS	CMOS	OFF
2/3	0	LVDS	LVDS	OFF
1	0	LVDS	CMOS	OFF
0	1/3	CMOS	CMOS	CMOS
1/3	1/3	LVDS	LVDS	LVDS
2/3	1/3	LVDS	LVDS	CMOS
1	1/3	CMOS	CMOS	LVDS
0	2/3	OFF	OFF	OFF
1/3	2/3	OFF	OFF	LVDS
2/3	2/3	OFF	OFF	CMOS
1	2/3	OFF	CMOS	OFF
0	1	LVDS	OFF	CMOS
1/3	1	CMOS	OFF	LVDS
2/3	1	LVDS	OFF	LVDS
1	1	CMOS	OFF	CMOS

Table 13. OUT2 Delay or Phase

S3	S4	OUT2 Delay (S0 ≠ 0)	OUT2 Phase (S0 = 0)
0	0	0	0
1/3	0	1/16	1
2/3	0	1/8	2
1	0	3/16	3
0	1/3	1/4	4
1/3	1/3	5/16	5
2/3	1/3	3/8	6
1	1/3	7/16	7
0	2/3	1/2	8
1/3	2/3	9/16	9
2/3	2/3	5/8	10
1	2/3	11/16	11
0	1	3/4	12
1/3	1	13/16	13
2/3	1	7/8	14
1	1	15/16	15

Table 14. OUT2 Divide or OUT1 Phase

S5	S6	OUT2 Divide (Duty Cycle[1]) (S2 ≠ 0)	OUT1 Phase (S2 = 0)
0	0	1	0
1/3	0	2 (50%)	1
2/3	0	3 (33%)	2
1	0	4 (50%)	3
0	1/3	5 (40%)	4
1/3	1/3	6 (50%)	5
2/3	1/3	8 (50%)	6
1	1/3	9 (44%)	7
0	2/3	10 (50%)	8
1/3	2/3	12 (50%)	9
2/3	2/3	15 (47%)	10
1	2/3	16 (50%)	11
0	1	18 (50%)	12
1/3	1	24 (50%)	13
2/3	1	30 (50%)	14
1	1	32 (50%)	15

[1] Duty cycle is the clock signal high time divided by the total period.

Table 15. OUT1 Divide or OUT2 Phase

S7	S8	OUT1 Divide (Duty Cycle[1]) (S2 ≠ 1)	OUT2 Phase (S2 = 1 and S0 ≠ 0)
0	0	1	0
1/3	0	2 (50%)	1
2/3	0	3 (33%)	2
1	0	4 (50%)	3
0	1/3	5 (40%)	4
1/3	1/3	6 (50%)	5
2/3	1/3	8 (50%)	6
1	1/3	9 (44%)	7
0	2/3	10 (50%)	8
1/3	2/3	12 (50%)	9
2/3	2/3	15 (47%)	10
1	2/3	16 (50%)	11
0	1	18 (50%)	12
1/3	1	24 (50%)	13
2/3	1	30 (50%)	14
1	1	32 (50%)	15

[1] Duty cycle is the clock signal high time divided by the total period.

Table 16. OUT0 Divide or OUT2 Divide

S9	S10	OUT0 Divide (Duty Cycle[1]) S2 ≠ 2/3	OUT2 Divide (Duty Cycle[1]) S2 = 2/3
0	0	1	7 (43%)
1/3	0	2 (50%)	11 (45%)
2/3	0	3 (33%)	13 (46%)
1	0	4 (50%)	14 (50%)
0	1/3	5 (40%)	17 (47%)
1/3	1/3	6 (50%)	19 (47%)
2/3	1/3	8 (50%)	20 (50%)
1	1/3	9 (44%)	21 (48%)
0	2/3	10 (50%)	22 (50%)
1/3	2/3	12 (50%)	23 (48%)
2/3	2/3	15 (47%)	25 (48%)
1	2/3	16 (50%)	26 (50%)
0	1	18 (50%)	27 (48%)
1/3	1	24 (50%)	28 (50%)
2/3	1	30 (50%)	29 (48%)
1	1	32 (50%)	31 (48%)

[1] Duty cycle is the clock signal high time divided by the total period.

DIVIDER PHASE OFFSET

The phase offset of OUT1 and OUT2 can be selected (see Table 13 to Table 15). This allows the relative phase of the outputs to be set.

After a SYNC operation (see the Synchronization section), the phase offset word of each divider determines the number of input clock (CLK) cycles to wait before initiating a clock output edge. By giving each divider a different phase offset, output-to-output delays can be set in increments of the fast clock period, t_{CLK}.

Figure 24 shows four cases, each with the divider set to divide = 4. By incrementing the phase offset from 0 to 3, the output is offset from the initial edge by a multiple of t_{CLK}.

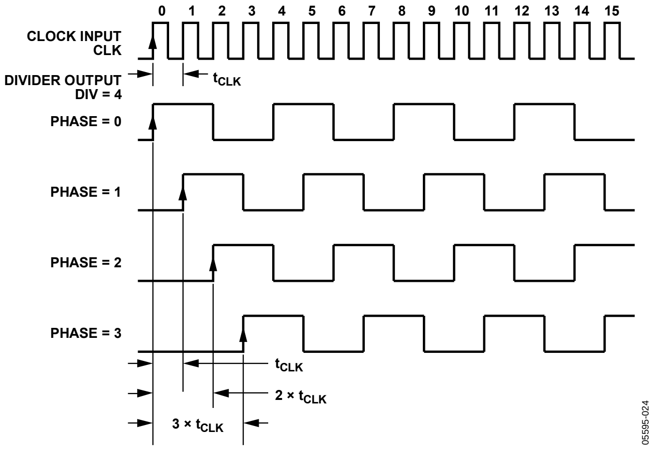


Figure 24. Phase Offset—Divider Set for Divide = 4, Phase Set from 0 to 2

For example:

CLK = 491.52 MHz

t_{CLK} = 1/491.52 = 2.0345 ns

For Divide = 4:

Phase Offset 0 = 0 ns

Phase Offset 1 = 2.0345 ns

Phase Offset 2 = 4.069 ns

Phase Offset 3 = 6.104 ns

The outputs can also be described as:

Phase Offset 0 = 0°

Phase Offset 1 = 90°

Phase Offset 2 = 180°

Phase Offset 3 = 270°

Setting the phase offset to Phase = 4 results in the same relative phase as Phase = 0° or 360°.

The resolution of the phase offset is set by the fast clock period (t_{CLK}) at CLK. The maximum unique phase offset is less than the divide ratio, up to a phase offset of 15.

Phase offsets can be related to degrees by calculating the phase step for a particular divide ratio:

Phase Step = 360°/*Divide Ratio*

Using some of the same examples:

Divide = 4

Phase Step = 360°/4 = 90°

Unique Phase Offsets in Degrees Are Phase = 0°, 90°, 180°, 270°

Divide = 9

Phase Step = 360°/9 = 40°

Unique Phase Offsets in Degrees Are Phase = 0°, 40°, 80°, 120°, 160°, 200°, 240°, 280°, 320°

DELAY BLOCK

OUT2 includes an analog delay element that gives variable time delays (ΔT) in the clock signal passing through that output.

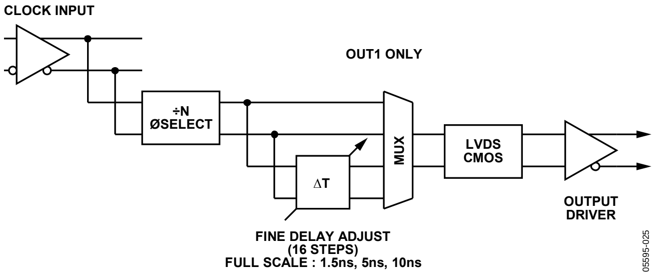


Figure 25. Analog Delay Block

The amount of delay that can be used is determined by the output frequency. The amount of delay is limited to less than one-half cycle of the clock period. For example, for a 10 MHz clock, the delay can extend to the full 11.6 ns maximum. However, for a 100 MHz clock, the maximum delay is less than 5 ns (or half of the period).

The AD9513 allows for the selection of three full-scale delays, 1.8 ns, 6.0 ns, and 11.6 ns, set by delay full-scale (see Table 11). Each of these full-scale delays can be scaled by 16 fine adjustment values, which are set by the delay word (see Table 13).

The delay block adds some jitter to the output. This means that the delay function should be used primarily for clocking digital chips, such as FPGA, ASIC, DUC, and DDC, rather than for supplying a sample clock for data converters. The jitter is higher for longer full scales because the delay block uses a ramp and trip points to create the variable delay. A longer ramp means more noise has a chance of being introduced.

When the delay block is OFF (bypassed), it is also powered down.

OUTPUTS

Each of the three AD9513 outputs can be selected either as LVDS differential outputs or as pairs of CMOS single-ended outputs. If selected as CMOS, the OUT is a noninverted, single-ended output, and OUTB is an inverted, single-ended output.

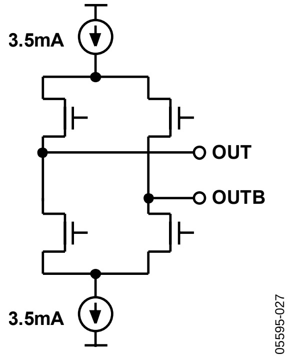


Figure 26. LVDS Output Simplified Equivalent Circuit

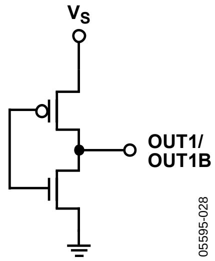


Figure 27. CMOS Equivalent Output Circuit

POWER SUPPLY

The AD9513 requires a 3.3 V ± 5% power supply for V_S. The tables in the Specifications section give the performance expected from the AD9513 with the power supply voltage within this range. In no case should the absolute maximum range of −0.3 V to +3.6 V, with respect to GND, be exceeded on Pin VS.

Good engineering practice should be followed in the layout of power supply traces and the ground plane of the PCB. The power supply should be bypassed on the PCB with adequate capacitance (>10 μF). The AD9513 should be bypassed with adequate capacitors (0.1 μF) at all power pins as close as possible to the part. The layout of the AD9513 evaluation board (AD9513/PCB) is a good example.

Exposed Metal Paddle

The exposed metal paddle on the AD9513 package is an electrical connection, as well as a thermal enhancement. For the device to function properly, the paddle must be properly attached to ground (GND).

The exposed paddle of the AD9513 package must be soldered down. The AD9513 must dissipate heat through its exposed paddle. The PCB acts as a heat sink for the AD9513. The PCB attachment must provide a good thermal path to a larger heat dissipation area, such as a ground plane on the PCB. This requires a grid of vias from the top layer down to the ground plane (see Figure 28).The AD9513 evaluation board (AD9513/PCB)provides a good example of how the part should be attached to the PCB.

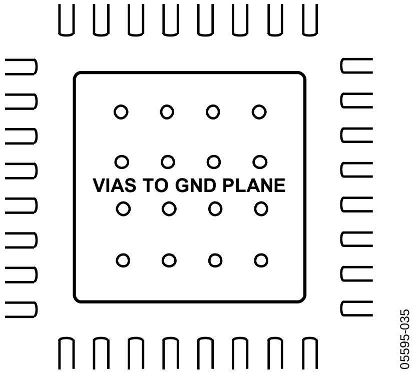


Figure 28. PCB Land for Attaching Exposed Paddle

POWER MANAGEMENT

In some cases, the AD9513 can be configured to use less power by turning off functions that are not being used.

The power-saving options include the following:

- A divider is powered down when set to divide = 1 (bypassed).
- Adjustable delay block on OUT2 is powered down when in off mode (S0 = 0).
- An unneeded output can be powered down (see Table 12). This also powers down the divider for that output.

APPLICATIONS

USING THE AD9513 OUTPUTS FOR ADC CLOCK APPLICATIONS

Any high speed, analog-to-digital converter (ADC) is extremely sensitive to the quality of the sampling clock provided by the user. An ADC can be thought of as a sampling mixer; any noise, distortion, or timing jitter on the clock is combined with the desired signal at the A/D output. Clock integrity requirements scale with the analog input frequency and resolution, with higher analog input frequency applications at ≥14-bit resolution being the most stringent. The theoretical SNR of an ADC is limited by the ADC resolution and the jitter on the sampling clock. Considering an ideal ADC of infinite resolution where the step size and quantization error can be ignored, the available SNR can be expressed approximately by

$$SNR = 20 \times \log\left[\frac{1}{2\pi f t_j}\right]$$

where *f* is the highest analog frequency being digitized.

t_j is the rms jitter on the sampling clock.

Figure 29 shows the required sampling clock jitter as a function of the analog frequency and effective number of bits (ENOB).

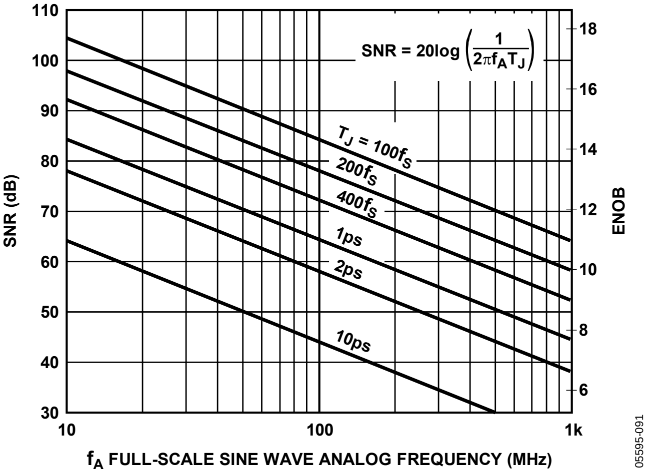


Figure 29. ENOB and SNR vs. Analog Input Frequency

See Application Note AN-756 and Application Note AN-501 at www.analog.com.

Many high performance ADCs feature differential clock inputs to simplify the task of providing the required low jitter clock on a noisy PCB. (Distributing a single-ended clock on a noisy PCB can result in coupled noise on the sample clock. Differential distribution has inherent common-mode rejection that can provide superior clock performance in a noisy environment.) The AD9513 features LVDS outputs that provide differential clock outputs, which enable clock solutions that maximize converter SNR performance. The input requirements of the ADC (differential or single-ended, logic level, termination) should be considered when selecting the best clocking/converter solution.

LVDS CLOCK DISTRIBUTION

The AD9513 provides three clock outputs that are selectable as either CMOS or LVDS levels. LVDS uses a current mode output stage. The current is 3.5 mA, which yields 350 mV output swing across a 100 Ω resistor. The LVDS outputs meet or exceed all ANSI/TIA/EIA-644 specifications.

A recommended termination circuit for the LVDS outputs is shown in Figure 30.

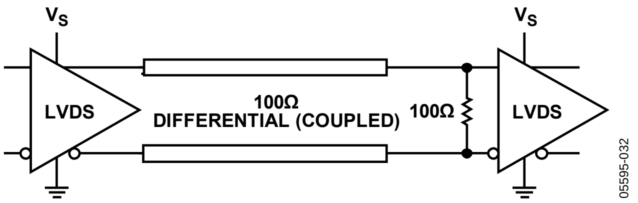


Figure 30. LVDS Output Termination

See Application Note AN-586 at www.analog.com for more information on LVDS.

CMOS CLOCK DISTRIBUTION

The AD9513 provides three outputs that are selectable as either CMOS or LVDS levels. When selected as CMOS, an output provides for driving devices requiring CMOS level logic at their clock inputs.

Whenever single-ended CMOS clocking is used, some of the following general guidelines should be used.

Point-to-point nets should be designed such that a driver has one receiver only on the net, if possible. This allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the net. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver. The value of the resistor is dependent on the board design and timing requirements (typically 10 Ω to 100 Ω is used). CMOS outputs are also limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 3 inches are recommended to preserve signal rise/fall times and preserve signal integrity.

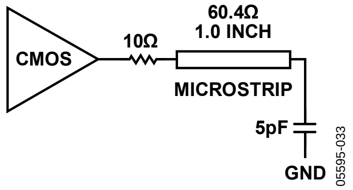


Figure 31. Series Termination of CMOS Output

Termination at the far end of the PCB trace is a second option. The CMOS outputs of the AD9513 do not supply enough current to provide a full voltage swing with a low impedance resistive, far-end termination, as shown in Figure 32. The far-end termination network should match the PCB trace impedance and provide the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

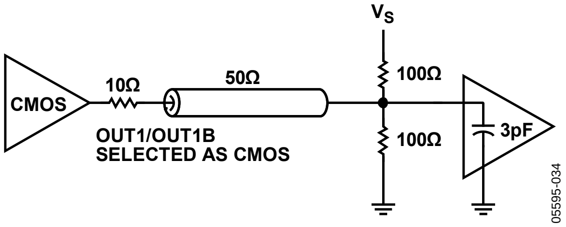


Figure 32. CMOS Output with Far-End Termination

Because of the limitations of single-ended CMOS clocking, consider using differential outputs when driving high speed signals over long traces. The AD9513 offers LVDS outputs that are better suited for driving long traces where the inherent noise immunity of differential signaling provides superior performance for clocking converters.

SETUP PINS (S0 TO S10)

The setup pins that require a logic level of ⅓ V_S (internal self-bias) should be tied together and bypassed to ground via a capacitor.

The setup pins that require a logic level of ⅔ V_S should be tied together, along with the VREF pin, and bypassed to ground via a capacitor.

POWER AND GROUNDING CONSIDERATIONS AND POWER SUPPLY REJECTION

Many applications seek high speed and performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the PCB is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing, as well as power supply bypassing and grounding to ensure optimum performance.

PHASE NOISE AND JITTER MEASUREMENT SETUPS

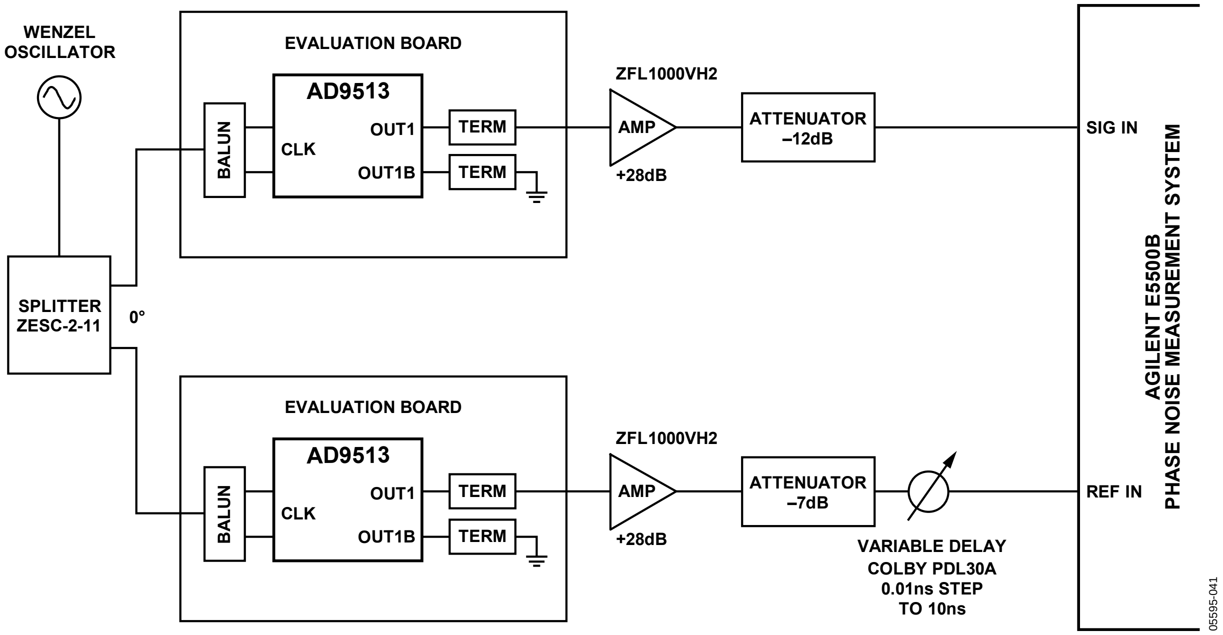


Figure 33. Additive Phase Noise Measurement Configuration

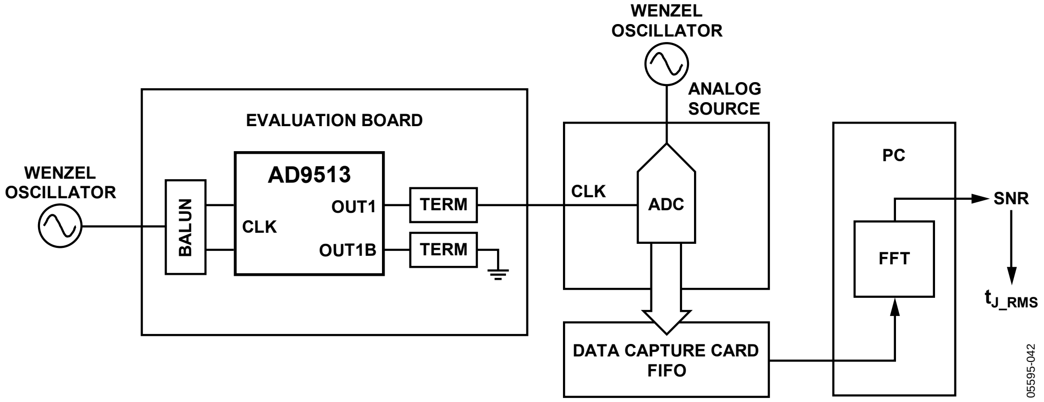


Figure 34. Jitter Determination by Measuring SNR of ADC

$$t_{J\_RMS} = \sqrt{\frac{\left[\dfrac{V_{A\_RMS}}{10^{\frac{SNR}{20}}}\right]^2 - \left(SND \times \sqrt{BW}\right)^2 - \left(\theta_{QUANTIZATION}{}^2 + \theta_{THERMAL}{}^2 + \theta_{DNL}{}^2\right)}{\left[2\pi \times f_A \times V_{A\_PK}\right]^2}}$$

where:

t_{j_RMS} is the rms time jitter.

SNR is the signal-to-noise ratio.

SND is the source noise density in nV/√Hz.

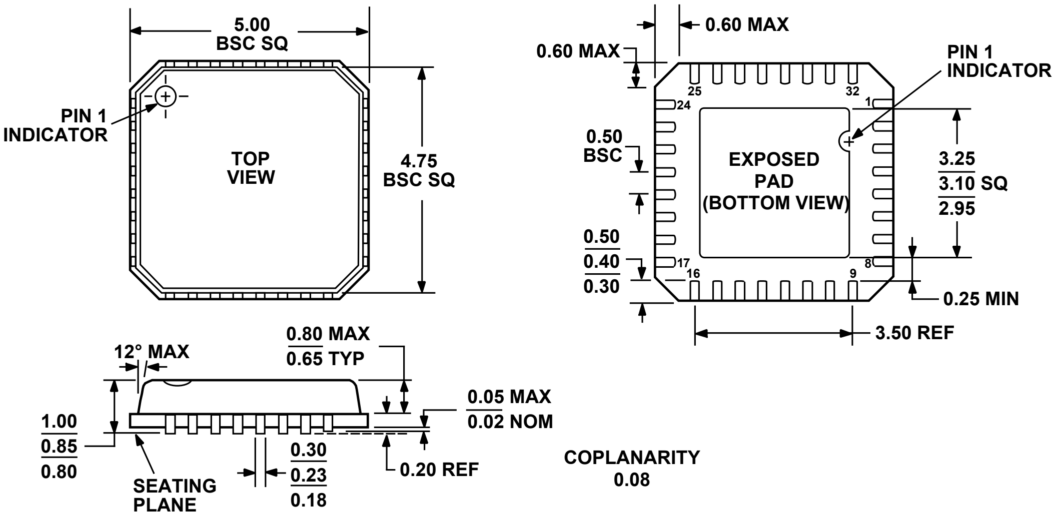
BW is the SND filter bandwidth.

V_A is the analog source voltage.

f_A is the analog frequency.

The θ terms are the quantization, thermal, and DNL errors.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

*Figure 35. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad (CP-32-2)
Dimensions shown in millimeters*

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9513BCPZ[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9513BCPZ-REEL7[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9513/PCB		Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

D05595–0–9/05(0)